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	Application No.	Applicant(s)
Notice of Allowability	10/718,515	YAMAMOTO, KENJI
	Examiner	Art Unit
	Sun J. Lin	2825
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308. 1. This communication is responsive to Amendments & Remarks filed on 03/03/2006.		
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2. The allowed claim(s) is/are 4-9,11-15 and 17-19, renumbered (37 CFR 1.126).		
3.		
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview Summary Paper No./Mail Da 98), 7. ⊠ Examiner's Amenda	

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Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Applicant's attorney David A. Blumenthal gave authorization for this examiner's amendment on May 16, 2006. The application has been amended based on Amendment filed on 03/03/2006 to correct some informalities as listed follows:

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Claim 11, line 11, change "formed as" to —formed of—.
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Claim 11, line 13 – 14, change "formed as" to —formed of—.

Claim 11, line 15, change "formed as" to —formed of—.

Claim 13, line 4, change "formed as" to —formed of—.

Claim 13, line 5, change "formed as" to —formed of—.

Claim 14, line 4, change "formed as" to —formed of—.

Claim 14, line 6, change "formed as" to —formed of—.

Claim 14, line 10, change "formed as" to —formed of—.

Claim 14, line 12, change "formed as" to —formed of—.

Claim 14, line 14, delete —and—.

Claim 14, line 11, change "formed as" to —formed of—.

Claim 14, line 15, change "formed as" to —formed of—.

Claim 14, line 15, delete —each of—.

Claim 14, line 16, change "second via" to —third via—.

Claim 14, line 16 – 17, change "second wiring;" to —third wiring; and—.

Claim 14, line 18 – 19, change "said fourth via being ...with said third via." to — Wherein:

said fourth via being supplied with one of a power potential and a third clock signal and being free from connection with said second via; and said upper-level wiring layer is formed as a customized wiring layer such that a pattern of said upper-layer wiring layer is determined based on customer specifications, and said lower-level wiring layer being formed as a fixed wiring layer such that a pattern of said lower-layer wiring is

determined independently of the customer specifications.—.

Claim 15, line 1, change "third via" to —fourth via—.

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Claim 15, line 2, change "to supply said second clock to said circuit" to —to be supplied with said third clock signal—.

Claim 16 is cancelled.

Claim 18, line 4, change "formed as" to —formed of—.

Claim 18, line 6, change "formed as" to —formed of—.

Claim 19, line 2, change "formed as" to —formed of—.

Reasons for Allowance

Claims 4 - 9, 11 - 15 and 17 - 19 are allowed over the prior art of record. An examiner's statement of reasons for allowance is given in the following:

Claims 4 - 9, 11 - 15 and 17 - 19 are allowed because the prior art doest not teach or fairly suggest the following subject matter:

- A master slice semiconductor integrated circuit <u>comprising at least two wiring layers for wiring and a plurality of clock buffer connected by clock wirings in a form of clock tree, wherein each of said clock wirings among said plurality of clock buffers comprises a wiring layer switching portion which switches a clock wiring from a lower wiring layer of said at least two wiring layers to an upper wiring layer of said at least two wiring layers wherein said upper wiring layer is a wiring layer for customized wirings, and said lower wiring layer is a wiring layer for fixed wirings in combination with other limitations recited in independent Claim 4;</u>
- A semiconductor device <u>comprising a first wiring layer above a semiconductor substrate</u>, <u>said first wiring layer being formed as a customized wiring layer such that a pattern of said first wiring layer is determined based on custom specifications</u> and <u>a second wiring layer between the semiconductor substrate and said first wiring layer</u>, <u>said second wiring layer being formed as a fixed wiring layer such that a pattern of said second wiring layer is determined independently of the customer specifications</u> in combination with other limitations recited in independent Claim 11;
- A semiconductor device having a multilevel wiring structure including a lower-level wiring layer, an upper-level wiring layer and an insulating film intervening between said lower-level and upper-level wiring layer, <u>said upper-level wiring layer is formed as a customized wiring layer such that a pattern of said upper-layer wiring layer is determined based on customer specifications, and said
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<u>lower-level wiring layer being formed as a fixed wiring layer such that a</u>
<u>pattern of said lower-layer wiring is determined independently of the customer</u>
<u>specifications</u> in combination with other limitations recited in independent

Claim 14.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday to Friday from 9:00am to 6:00pm.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun J. Lin Patent Examiner Art Unit 2825 May 17, 2006

> SUN JAMES LIN PRIMARY EXAMINER